Proc. IEEE Applied Power Electronics Conference (APEC), 1997

Switched Capacitor System for Automatic Series Battery Equalization

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Abstract—A clocked switched-capacitor circuit can exchange charge between adjacent batteries in a series string. This exchange drives all batteries to identical voltages, without regard to component values, battery technology, or state of charge. This equalization process can proceed while the batteries are in use or under charge, or separately. Transformer-based and transformerless implementations are given, and results of experimental tests are provided. The process is much faster and less stressful than the conventional approach, and is simpler than some recent active approaches.

I. INTRODUCTION

Series strings of storage batteries are used by the million in the telephone industry, the utility industry, in military applications, in portable tools and appliances, in power backup, and in electric vehicles. If the series string is charged as a unit, slight mismatches or temperature differences cause charge imbalance, in the form of unequal voltages along the string. Once imbalance occurs, it tends to grow with time: low batteries charge less effectively, and high batteries charge relatively quickly. Charge equalization cycles must be used in an attempt to correct imbalance, but conventional approaches to this process stress the batteries, shorten their life, and are not always effective.

This paper describes a switched-capacitor approach to battery equalization. A group of capacitors is used to shift charge among adjacent batteries in a string. When the capacitors are switched back and forth repeatedly, they bring the battery voltages in an arbitrarily long series string to exactly equal values. The equality is independent of capacitor value, switching speed, component values, and even battery chemistry. A block schematic of the concept is given in Fig. 1. The switches operate together, and connect alternately to each upper and lower contact point. The switching function shows the action: high for the upper contact and low for the lower contact. The center position of the clock signal sets a dead time to avoid any possibility of shoot through during the process. Through this simple action, charge is transferred from higher voltage levels to lower levels. After a time, each battery carries identical voltage. The equalizer uses single-pole double-throw switches. A transformer-coupled MOSFET set is one way to implement such a such, and this SPDT function is shown at the bottom of the figure.

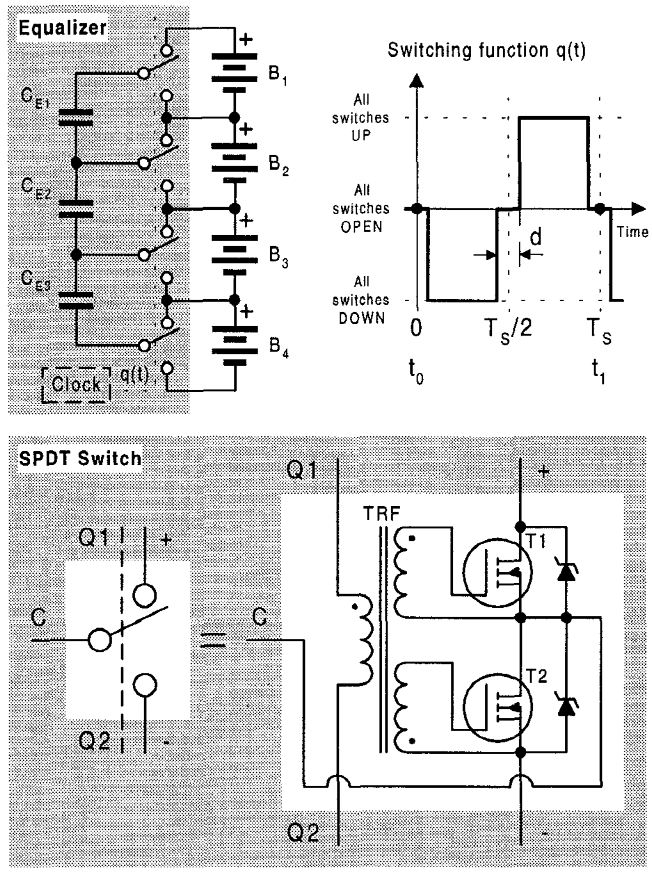

Fig. 1. Block diagram of switched capacitor equalizer, with single synchronized control. Top left: system layout. Top right: switching function. Bottom: details of one form of SPDT switch implementation.

II. PREVIOUS METHODS

Users of battery strings have long been aware of the charge imbalance problems associated with series charging. During the charging process, an imbalance means that some cells are undercharged while others are overcharged. The operation of a series string is limited by the weakest cell. Even a few tens of millivolts of imbalance will tend to alter the charge process so that imbalance increases over time.

In practice, equalization must be done periodically to avoid severe long-term imbalance. Equalization is most often performed with extended charging. The highest cells are forcibly overcharged while the lowest ones are brought up to

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full charge. This is presumed to work because overcharging sets up a nonlinear hydrolysis process, and provides a way for low-voltage cells to "catch up." In most technologies, the overcharge evolves hydrogen gas and removes water from the highest cells. Even when hydrogen recovery catalysts are present, over repeated cycles, side reactions and the loss of water degrade the performance and shorten the useful life.

The deliberate charging extension method can be termed *passive equalization*. In the literature, active equalization methods have been proposed in the past few years. In [1], three alternatives are described. The first diverts charging current around high batteries. Conceptually, this is equivalent to a parallel Zener diode connected to limit the voltage. This process causes energy loss, and can be used only when efficiency is not important. The second uses a set of power converters to send charge selectively to weaker cells. A multi-output forward or flyback converter can perform this function -- if the outputs are matched precisely. The third uses a set of power converters to divert charge away from stronger batteries, but returns the energy to the entire series string with minimal loss. The first method is impractical in commercial applications since excess charge is dissipated as heat. The second and third require precise control to match battery voltages in a long string.

One approach now under development [2,3] is based on the second active method above. This technique uses a coaxial transformer to provide accurate matching. The tolerance issues and costs associated with this approach are significant drawbacks. Another approach [4] addresses the third active method. In effect, individual switching power converters are provided for each battery. This has limited practical value in long strings, because of cost and component mismatch. A key limitation of all these methods, both passive and active, is that they function only at the end of the charge process, after at least one battery is fully charged.

III. The Switched Capacitor Approach

A. Properties

The switched capacitor approach performs equalization on the same time scales as active methods if the switching frequency is selected properly. The capacitor value is not relevant to the final result, but only to the rate of charge exchange. The switching process is not critical, except that it must be fast, and the switches must exhibit no voltage drop as the current decreases to zero. The method can be extended to long series strings or to individual cells without limit. Given *n* batteries in series, a string of *n*-1 capacitors is switched back and forth between a low connection and a high one. The full capacitor string "diffuses" imbalanced charge until all batteries match. Conventional power MOSFETs meet the requirements for the switch hardware. Each switch needs to block only the voltage of a single battery -- rarely more than 15 V. The capacitors also require only 15 V ratings. Appropriate values will be in the range of 20 μF to 1000 μF.

B. Advantages

Key advantages of the new approach over existing methods include:

1) Precise equalization is performed without any requirements for device matching or tight tolerances.

2) No sensing or closed-loop control are needed.

3) An identical implementation can be used for lead-acid batteries, nickel-cadmium batteries, nickel-metal-hydride batteries, or other conventional rechargeable chemistries. No change or recalibration will be necessary. The method extends to equalization of individual cells as well as to complete batteries.

4) The concept is modular, and extends to arbitrary numbers of batteries. It would not matter if modules for different batteries have different values of capacitance or use different MOSFETs.

5) The equalization process can be performed during the main charging process, separately, or continuously during battery operation with minimal power drain. Equalization takes place without regard to level of charge.

6) The process does not interfere with safety or protection systems. Since charge is exchanged rather than delivered, very little energy is manipulated at any given time within the equalization circuits.

7) The process is self-limiting. When equalization is complete, continued switching of the capacitors consumes minimal energy, exchanges no charge, and has no further effect.

IV. Mathematical Analysis

A model has been developed to analyze and predict the behavior of the system. The simplest model for a battery is a capacitor, with a value C_B proportional to the capacity. For testing purposes, industry-standard U1 lead-acid batteries have been used. The tested batteries are rated at 12 V, 32 A·h, and the corresponding value of C_B is approximately 50 kF. Each MOSFET is modeled as an ideal switch in series with a resistor R_{ON}. The capacitors in the equalization string are denoted as C_E. Fig. 2 shows the resulting circuit model for the case of four batteries.

The exponential action that governs every half switching period can be determined, then used to build discrete-time equations. Discrete-time instants $t_k = k \cdot T_S$ are shown as dots in the top right part of Fig. 1. Voltages across all capacitors are chosen as state variables. In the general case of *n* batteries, there will be *2n-1* state variables: *n* batteries plus *n-1* equalization capacitors. The state of the system at time t_k can be written as:

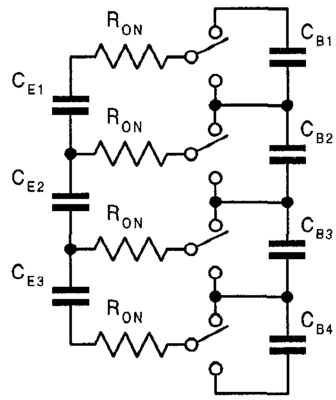

Fig. 2. Model of the equalizer for four batteries.

$$x_k = \left[V_{B1}^k \quad \cdots \quad V_{Bn}^k \;\vdots\; V_{E1}^k \quad \cdots \quad V_{E(n-1)}^k \right]^T .$$

One magnitude repeatedly used throughout this study is the DTP (dead time percentage), defined as:

$$DTP = \frac{2d}{T_S} \cdot 100\,\% .$$

The discrete-time equations predict the state of the system at time t_{k+1}, x_{k+1}, knowing any present state, x_k. In matrix form, $\boldsymbol{x}_{k+1} = \boldsymbol{A} \cdot \boldsymbol{x}_k$, where A is a $(2n\text{-}1)$ x $(2n\text{-}1)$ matrix with constant coefficients that are functions of C_B, C_E, R_{ON}, f_S and DTP. Given the initial state of the system, x_0, any future x_k can be found.

Computer simulations involving up to six batteries were run and their results match the equalizer performance measured in the laboratory, within the limitations of a simple capacitive battery model.

V. Implementation

As illustrated in Fig. 1, the switched capacitor equalizer admits straightforward implementation with transformers. This arrangement could use either a synchronized master clock, driving all primaries, or could use independent clocks controlling one pair of cells linking adjacent batteries. The transformer approach is a convenient way to construct equalizers when high isolation requirements are needed, or when it is desired to equalize within a battery on a cell-by-cell basis. This study, however, focuses on transformerless designs, in an attempt to reach extremely low power levels and to demonstrate a version that would lend itself to integration.

A. Block Diagram

Fig. 3 shows a block diagram of a transformerless equalizer version that has been built and tested. A single clock generator provides "up" and "down" phases P1 and P2. These signals excite one equalizer cell per battery. Capacitive coupling maintains isolation throughout the battery string. The equalizer cell circuits are identical, except the lowest one (the one closest to the clock generator). This will be called a Type I cell. Other cells will be called Type II. The first cell is different because it makes use of only positive voltages for MOSFET gating. Type II cells use both the negative and positive polarity of the clock phases to turn off and on, respectively, their corresponding switches. The equalization capacitors C_E are mounted within the cells.

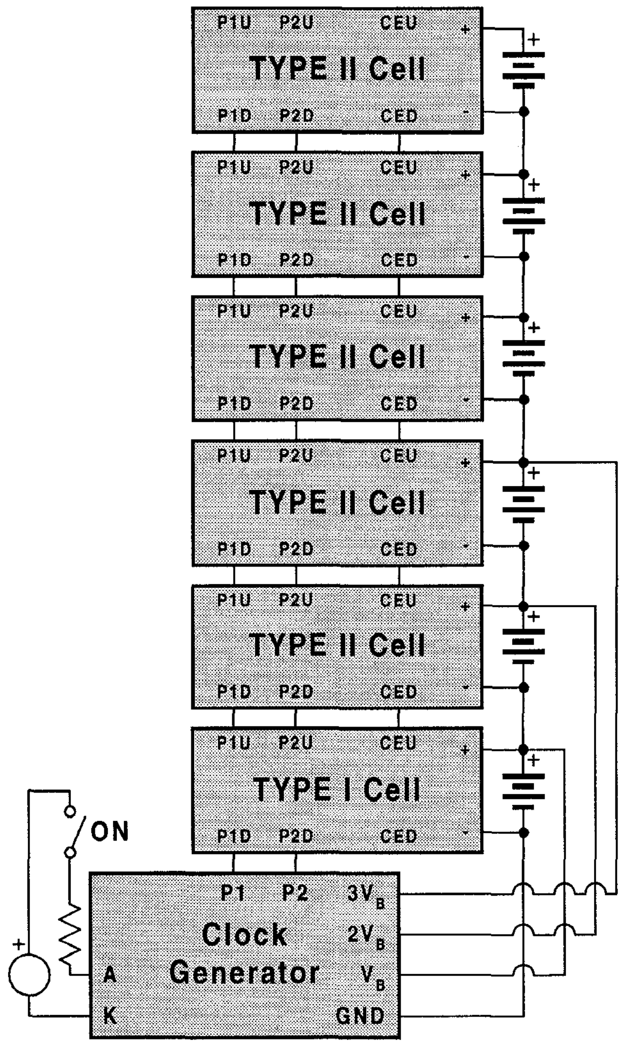

Fig. 3. Block diagram of the transformerless equalizer system.

The clock generator uses voltage V_B (with a range of 3 to 18 V), and also the double and the triple of that value in order to generate P1 (with a nominal amplitude of 36 V) and P2 (with a nominal amplitude of 24 V). The clock generator is provided with an optocoupled input with the function of turning on or off the entire equalizer. When a small current is injected into that input, the circuit operates. With no input current, the equalizer stops and stays in a high impedance state (as seen by the batteries), and the entire system consumes negligible quiescent power. Because of the optocoupler, this ON input is completely isolated from the batteries.

B. Equalizer Cells

Fig. 4 shows the details of the Type II equalizer cell. Component values are listed in Table I. Each SPDT (single-pole double-throw) switch in top left part of Fig. 1 has been split into two N-channel power MOSFETs to take advantage of the minimal ON resistance available in this technology. These transistors require a drain-to-source breakdown voltage of only about 20 V. Bipolar devices were rejected because of their nonzero saturation voltage.

C_E is the capacitor that redistributes the charge in the equalization process. C_{IN} filters the battery current and decouples any connection inductance. This helps make the equalization process more accurate and less dependent on the resistance of connecting wires. However, recent results in pulsed charging methods [5] suggest that C_{IN} might not be necessary.

The four zener diodes DZ_{1a}, DZ_{1b}, DZ_{2a} and DZ_{2b} (all with V_Z=15 V) protect the MOSFET gates.

If the P1 or P2 excitations are excessive and some zeners are conducting, it is important to have current-limiting resistors, shown as R_{Sx} and R_{Px} , between the excitation and the zeners. The speed-up capacitor C_{Px} is included so these resistors do not slow the gate charging process.

C_1 and C_2 belong to two strings of capacitors that couple the clock phases P1 and P2 into the equalizer cells. Diodes D_1 and D_2 maintain appropriate dc bias levels on these capacitors, and resistors R_{D1} and R_{D2} relieve any excess voltage that might appear because of noise, overshoot or spikes in the excitation waveforms.

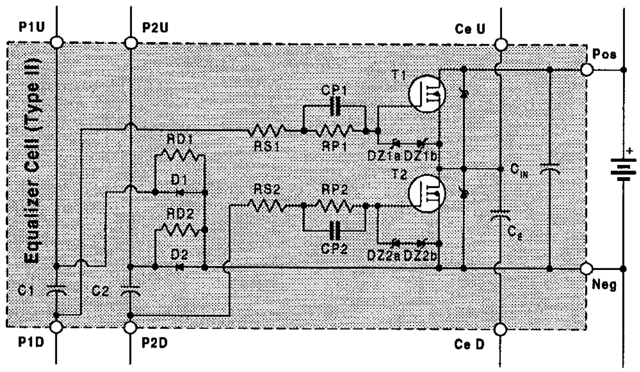

Fig. 4. Type II equalizer cell.

TABLE I
COMPONENT VALUES FOR TYPE I AND TYPE II EQUALIZER CELLS

RP1	10 KΩ	RD2	100 KΩ	DZ2a	1N4744A	C2	1 μF
RP2	10 KΩ	D1	1N4148	DZ2b	1N4744A	Ce	470 μF, 25V
RS1	100 Ω	D2	1N4148	CP1	1 μF	Cin	470 μF, 25V
RS2	100 Ω	DZ1a	1N4744A	CP2	1 μF	T1	MTP50N05EL
RD1	100 KΩ	DZ1b	1N4744A	C1	1 μF	T2	MTP50N05EL

Fig. 5 shows the Type I cell. The only difference from Type II cells is that capacitors C_1 and C_2, diodes D_1 and D_2, and resistors R_{D1} and R_{D2} are not needed. The values for the other components are exactly the same as in Table I.

C. Clock Generator

A block diagram and detailed schematic for the clock generator are shown in Fig. 6. Table II lists the component values. The circuit has been optimized for very low power consumption. Using standard CMOS integrated circuits, the entire V_B shaded area consumes only 2.90 mA at 12 V with 20 kHz switching. Most of the power consumed by the clock generator (and by the whole equalizer system) is dissipated in the drain resistors R_6, R_7, R_9 and R_{10}. The power could be reduced further by enforcing a dead time between the excitations of T_1 and T_2, and between those of T_3 and T_4, just as for the pairs of MOSFETs in each equalizer cell. However, consumption is very modest even without this precaution.

VI. EXPERIMENTAL RESULTS

A. Power Consumption

The system with one clock generator and two equalizer cells consumes 430 mW when attached to two 12 V batteries previously equalized. Fully 93% of this power is dissipated by the clock generator, so the power consumption of the system is not linearly proportional to the number of batteries. For setups involving over five batteries of the U1 size, the consumption per battery is actually smaller than the internal battery self-discharge power.

B. Equalization Process

The setup for the first experiment is sketched in Fig. 7, for the case of *n*=6 batteries. The equalizer and a power supply are simultaneously acting on the battery string. The parameters of the equalizer are f_S=20 kHz and DTP=10 %, and the power supply limits are set to V_{LIMIT}=84 V and

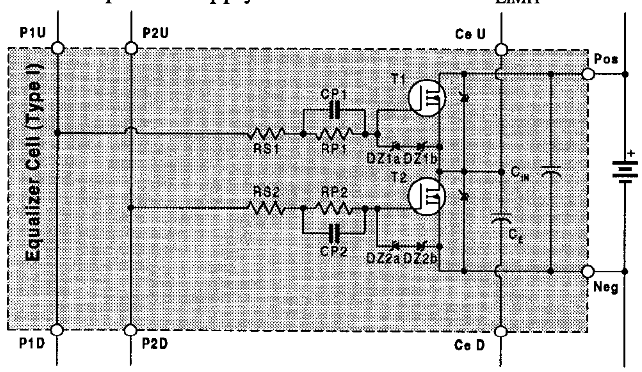

Fig. 5. Type I cell.

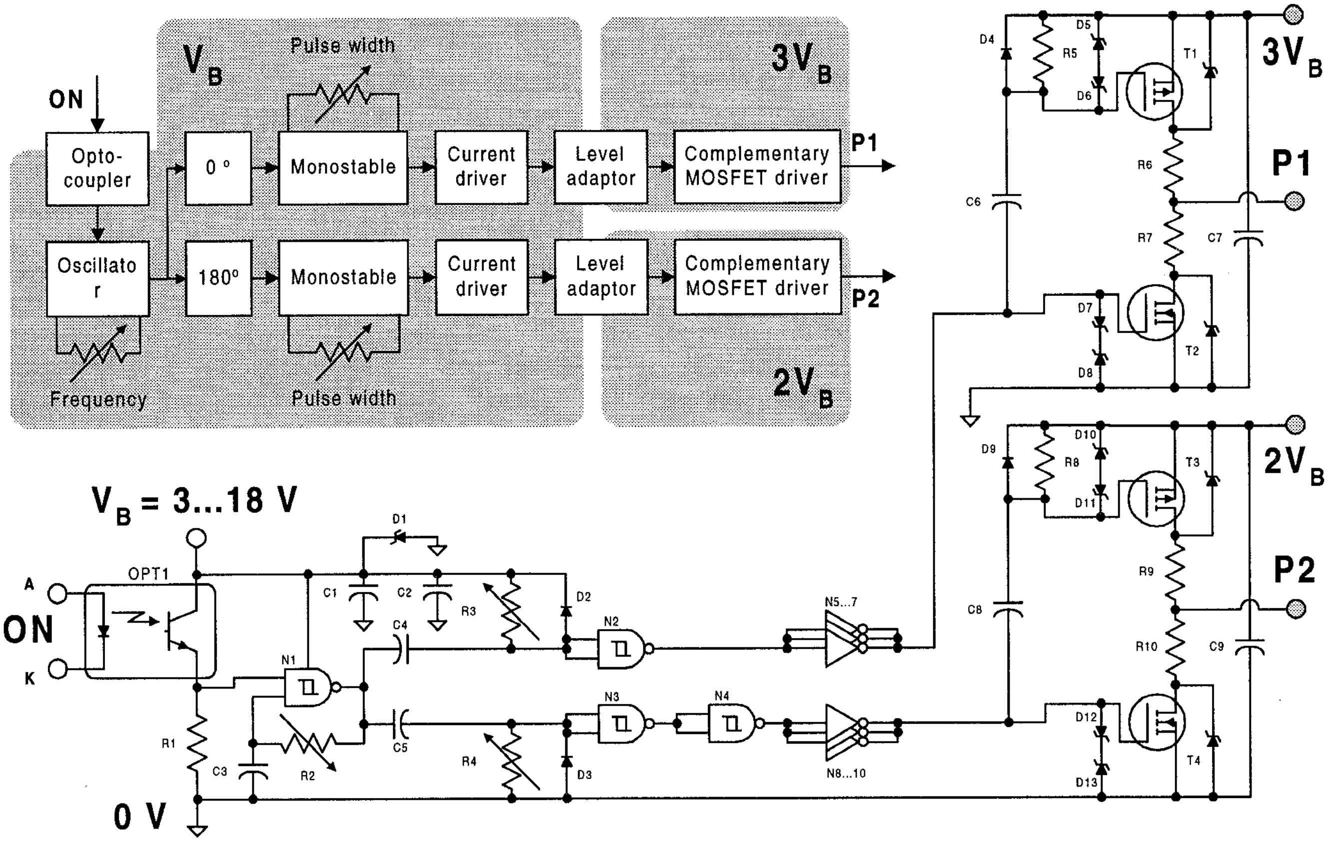

Fig. 6. Clock generator. Top: block diagram. Bottom: schematic circuit.

TABLE II
COMPONENT VALUES FOR THE CLOCK GENERATOR

R1	1 MΩ	C4	1.5 nF	D8	1N4744A (15 V)
R2	100 KΩ, adj	C5	1.5 nF	D9	1N4148
R3	100 KΩ, adj	C6	1 μF	D10	1N4744A (15 V)
R4	100 KΩ, adj	C7	1 μF	D11	1N4744A (15 V)
R5	100 KΩ	C8	1 μF	D12	1N4744A (15 V)
R6	10 Ω	C9	1 μF	D13	1N4744A (15 V)
R7	10 Ω	D1	1N4746A (18 V)	T1	IRF9510
R8	100 KΩ	D2	1N4148	T2	IRF510
R9	10 Ω	D3	1N4148	T3	IRF9510
R10	10 Ω	D4	1N4148	T4	IRF510
C1	470 μF, 25V	D5	1N4744A (15 V)	N1..4	CD4093B
C2	1 μF	D6	1N4744A (15 V)	N5..10	CD4049UB
C3	1.5 nF	D7	1N4744A (15 V)	OPT1	MCT2

I_{LIMIT}=1 A. Fig. 8 shows the evolution of the battery voltages vs. time. In this test, the power supply enforced constant current until the voltage limit was reached after about 10 h. Only the *total* voltage is limited by the power supply after that time, not the individual voltages. This figure shows that none of the voltages exceeds 14 V for a significant interval. This is equivalent to separately limiting each one of the individual voltages, i.e., equivalent to having separate power supplies dedicated to each battery. The equalizer avoids this dedicated supply approach, and enables the charging of the whole string of batteries through only two terminals. After about 20 h, the six batteries are equalized within about 50 mV.

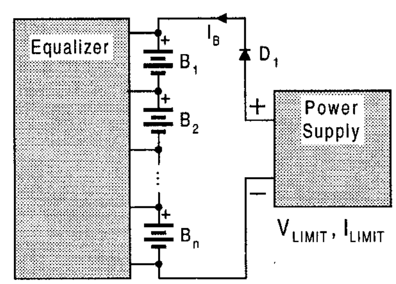

Fig. 7. Setup for the first experiment.

Fig. 9 shows the standard deviation of individual battery voltages during the equalization process. The standard deviation falls quickly at first, then enters a much slower regime. Thanks to the initial rapid decrease, the standard deviation is reduced from 0.5 V to 0.05 V in about 20 h. After that, the reduced speed is not a serious problem because the differences are already small.

The second experiment repeats the first one, but without employing any equalizer; only the charger is used. Most of the voltages in Fig. 10 rise above 14.5 V for lengthy intervals, and one battery approaches 15 V as the process evolves. This

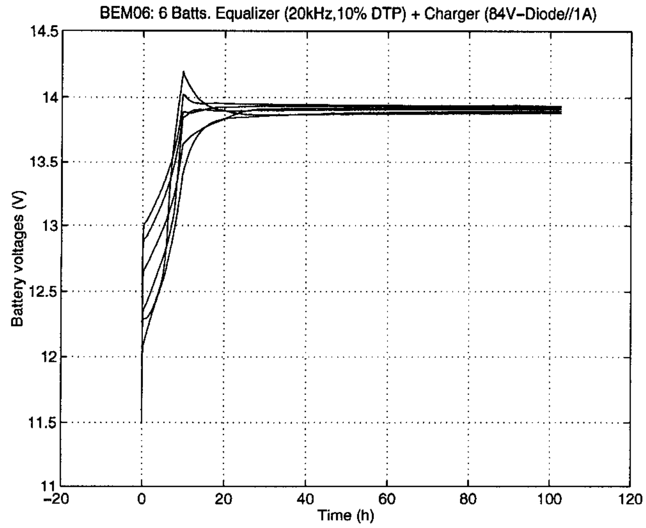

Fig. 8. First experiment. Battery voltages.

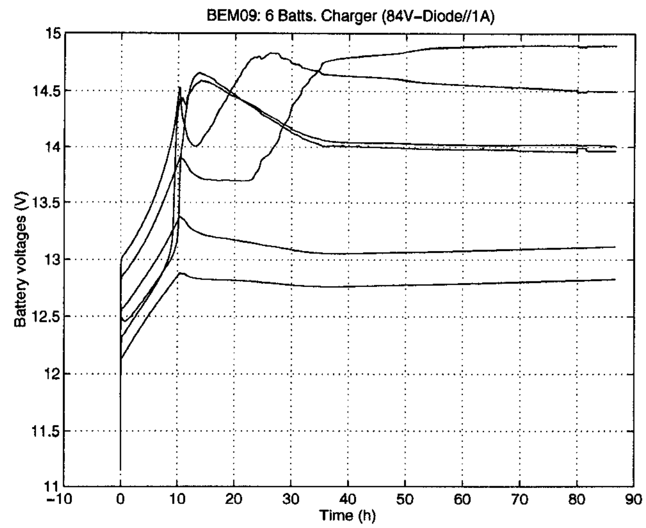

Fig. 10. Second experiment. Battery voltages.

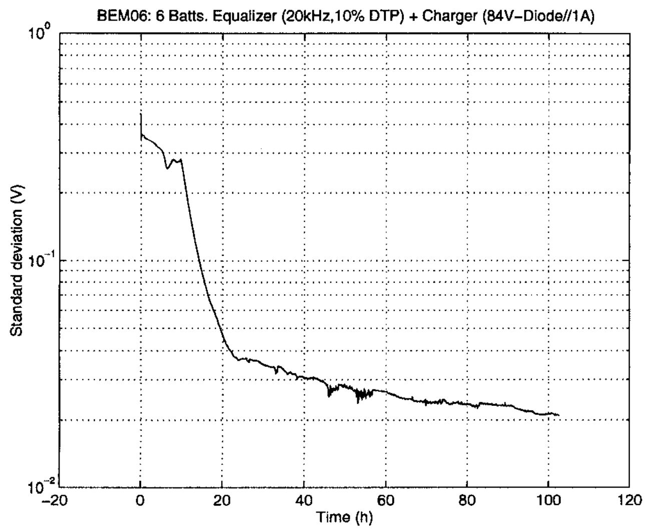

Fig. 9. First experiment. Standard deviation.

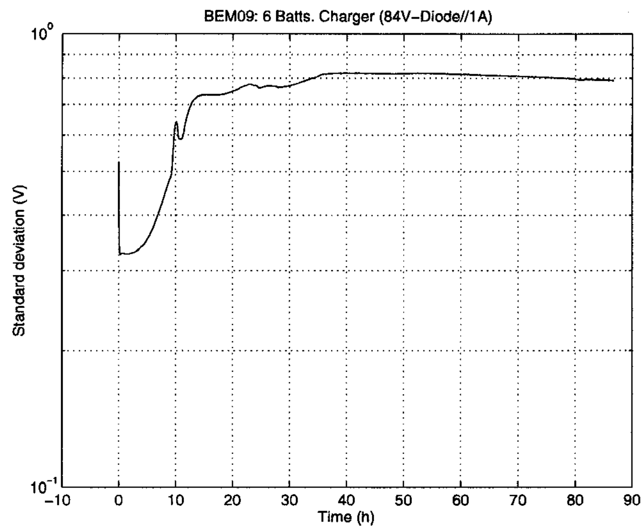

Fig. 11. Second experiment. Standard deviation.

test represents the conventional passive approach. The equalization time is vastly extended, and indeed the standard deviation shown in Fig. 11 calls into question whether the voltages are approaching each other even after 86 h. The batteries exposed to the highest voltages will lose water from the cells and their life will be reduced. It is slow, too. Increasing the value of I_{LIMIT} does not improve the situation, as the power supply behaves as a constant voltage source after t=10 h. Increasing V_{LIMIT} will only stress the high-voltage batteries even more. Comparing Fig. 10 to Fig. 8, it is clear that the switched-capacitor process is far more effective than passive equalization, without any of the complexity associated with multi-charger active systems.

VII. Conclusion

A switched capacitor equalizer for series strings of batteries has been developed and presented. Based on an elemental mechanism of charge redistribution, and implementable as an extremely simple circuit, it is capable of bringing the voltage differences to zero in a reasonable time. To accomplish its goal, no sensor or control technique is needed, and no part of the circuit requires calibration. The speed of action depends on design parameters, but the final equalized state does not. The working principle makes the system robust so wide-tolerance, low cost components are suitable, and most parts could be integrated into a single chip. The scheme is extendable to any type and number of batteries. The power requirement is minimal and not linearly proportional to the length of the series string.

A mathematical model has been developed and exploited, and a complete implementation for six batteries has been built and tested. The results show drastic improvement over passive equalization in terms of speed of operation and battery care, and the present proposal appears to be the simplest alternative among active equalization methods.

ACKNOWLEDGEMENT

This paper is based in part on an M.S. thesis by one of the authors (C. P.), submitted to the University of Illinois at Urbana-Champaign.

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